Model # BXFS1045

2-18 GHz Broadband Synthesizer

+13 dBm Output Power with Low Phase Noise

Features

- Ultra Low Phase Noise: - 81 dBc/Hz @ 10 KHz Offset
- Frequency control options include Serial inputs or BCD/Binary format.
- Fully Customizable
- Multiple Frequency Control Options
- Environmental Screening Available

Model BXFS1045 2-18 GHz Synthesizer covers the S, C, X, and Ku-Bands, offers fast 65 µsec settling time, provides +13 dBm of output power from the +/- 6 and +5 volt supply, and delivers low phase noise performance (-81 dBc/Hz @ 10 KHz Offset). API Technologies offers flexibility to meet customer-specific requirements including options for input voltages, output power, and frequency control.

Using a hermetic laser-welded package, the BXFS1045 is able to withstand extreme environmental conditions, and is configurable for most military airborne and ground based applications. Able to provide outstanding performance at a wide temperature range (-40°C to +85°C), the Synthesizer is ideally suited for military requirements and high-end commercial applications such as microwave receivers, microwave telemetry systems, uplink communication platforms, instrumentation, and military communication systems.

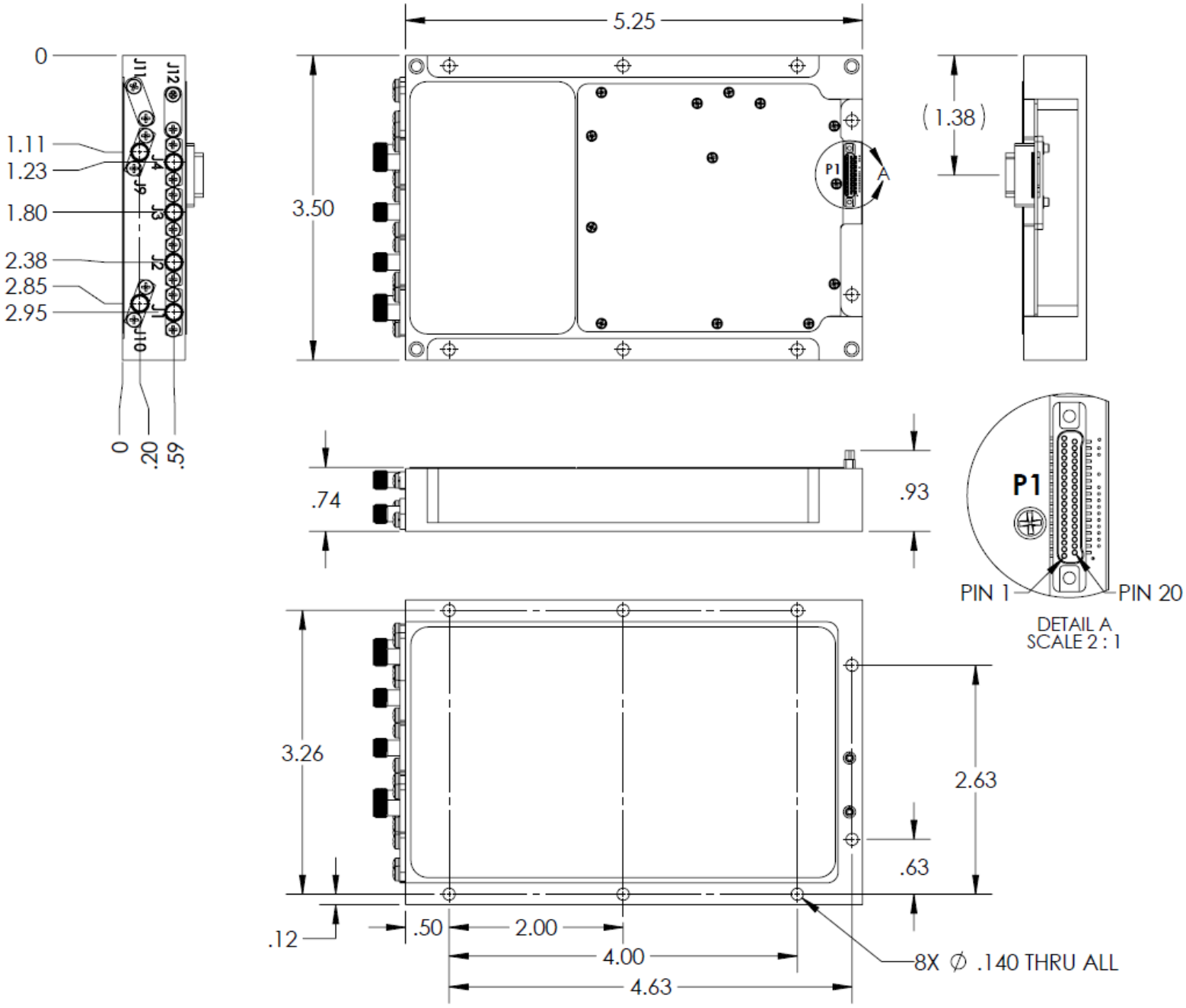
Technical Specifications

Parameter	Typical	Min/Max
Frequency Range	2 - 18 GHz	2 - 18 GHz
Output Power	13 dBm (x4)	-
Internal Input Reference Frequency	100 MHz	100 MHz
Step Size (at 18 GHz)	20 MHz	20 MHz
SSB Phase Noise (at 18 Ghz)	-80 dBc/Hz @ 1 kHz -81 dBc/Hz @ 10 kHz -82 dBc/Hz @ 100 kHz -113 dBc/Hz @ 1 MHz -135 dBc/Hz @ 10 MHz	-
Settling Time	65 µsec	-
Stability	+/- 10 ppm	-
Spurious	-60 dBc	-
Harmonics	-15 dBc	-
Sub-Harmonics	-25 dBc	-
Input/Output VSWR	2.0:1	2.5:1
DC Supply Voltage	+6 volts, + 5 volts, -6 volts	(+/- 2%)
DC Supply Current	650 mA, 300 mA, 50 mA	700 mA, 350 mA, 100 mA

Maximum Ratings

Minimum (No Damage) Results	
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +85°C
DC Voltage @ 25°C	8 Volts

Outline Drawing



Miscellaneous:

1. Specifications labeled “min.” or “max.” are guaranteed in a 50 Ohm system over the specified temperature range.
2. Higher output power is available.
3. Other input voltages are available.

Control

Power and Control connector P1 shall be a dual-row 37-pin Nano miniature plug IAW MIL-DTL-32139. The connector shall have a metal shell with Electroless nickel finish, and shall be a vertical SMT PC board mount style. A suggested part number is Airborn NK-2A2-037-225-TH00.

Table 2: Pin Assignments

P1 Pin	Signal Name
1	BIT_100 MHz_J10_Power
2	BIT_FREQ_Lock
3	FREQ latch-N
4	CH0 (LSB) / pwrdown-N
5	CH1 / FREQoff-N
6	CH2
7	CH3
8	CH4
9	CH5
10	CH6
11	CH7
12	CH8
13	CH9
14	CH10
15	CH11 (MSB)
16	Spare
17	Control latch-N
18	Spare
19	Spare
20	Ground
21	+6.0 VDC
22	+6.0 VDC
23	Ground
24	-6.0 VDC
25	Ground
26	Temp_Ground
27	Temp_SI/O
28	Temp_CS-N
29	Temp_SC
30	Temp_V+
31	Spare
32	BIT_RF_Power
33	Spare
34	Spare
35	BIT_100 MHz_J9_Power
36	Ground
37	+5.0 VDC
	Logic levels are LV (+3.3V TTL logic)

Temperature Sensor Signals **Temp_SI/O** **Temp_SC** **Temp_Ground** **Temp_CS-N** **Temp_V+**	**The subassembly shall use a 3-wire SPI-compatible local temperature sensor capable of running with a Vcc ranging from 3.0V to 5.5V. All 3 SPI interface pins (clock, data, and select) and the Vcc pin shall be wired out directly, and only, to the subassembly connector. The GND pin shall be wired out directly, and only, to the subassembly connector. This allows temperature to be read at all times regardless of power down state or other subassembly power inputs. Vcc shall be bypassed to GND with a 0.1uF capacitor. Part number MAX6630MUT is suggested (http://www.maxim-ic.com/datasheet/index.mvp/id/2577/t/al). This part is also available on tape & reel. If this part is used, it is suggested to connect pin 2 (NC) to ground through a provisional resistor (initially unpopulated) for compatibility with similar parts from other manufacturers.** **The temperature sensor interface signals will be static during RF measurements.**
BIT_Ref_J9_Power	**Power monitor for 100 MHz reference output J9. Output shall be logic "1" for output power > -5 dBm and logic "0" for output power < -10 dBm.**
BIT_Ref_J10_Power	**Power monitor for 100 MHz reference output J10. Output shall be logic "1" for output power > +10 dBm and logic "0" for output power < +5 dBm.**
BIT_FREQ_Lock	**Phase lock indicator for the synthesizer. Output shall be logic "1" when the synthesizer has achieved phase lock, and logic "0" otherwise.**
BIT_RF_Power	**Power monitor for the synthesizer. Output shall be logic "1" for J1, J2, J3, and J4 output power > +8 dBm and logic "0" for output power < +3 dBm.**
Spare	**Pins which are unused but reserved. To maintain compatibility with future designs, these pins shall be left unconnected.**

LVTTL Control Levels: Control inputs shall use 3.3V LVTTL logic levels. Each input shall source or sink 0.5mA maximum. LVTTL low, or logic '0', shall be 0.8 volts maximum. LVTTL high, or logic '1', shall be 2.0 volts minimum. Steady-state input voltage shall be 0.0 volts minimum and 3.5 volts maximum.

LVTTL Output Levels: Outputs shall use 3.3V LVTTL logic levels. LVTTL low, or logic '0', outputs shall be 0.5 volts maximum when sinking up to 2 mA. LVTTL high, or logic '1', outputs shall be 2.4 volts minimum when sourcing up to 2 mA. Steady-state output voltage shall be 0.0 volts minimum and 3.5 volts maximum.